

**EFFECTS OF COEFFICIENT OF THERMAL  
EXPANSION MISMATCH ON SOLDER ATTACHED GaAs MMICs**

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**ABSTRACT**

An evaluation/qualification was undertaken to examine reliability effects of GaAs solder attachment to a variety of different materials with a diverse range of coefficients of thermal expansion (CTE). Failure mechanisms included fractures or cracks through the devices as well as cracking of the corners. GaAs devices placed under tensile stress with materials such as Kovar (CTE 5.1 ppm/ $^{\circ}$ C) experienced severe cracking and corner fracture through long term reliability screening. Devices placed under compressive stress, on the other hand, did not degrade through life testing unless the CTE mismatch was greater than or equal to 16.5 ppm/ $^{\circ}$ C. From this evaluation, a coefficient of thermal expansion range was defined at which GaAs can be reliably attached and expected to operate without failures through 1000 cycles of MIL-STD thermal cycling.

**INTRODUCTION**

More extensive application of GaAs MMIC technology in military and commercial systems has led to development of an industry-wide, historical data base on the long term reliability of these assemblies. It has been noted that stress gradients developed during wafer and device processing have the potential to cause propagated fractures during subsequent assembly and/or environmental conditioning. These effects can become more severe depending on assembly configuration, on geometries of the devices, and, in particular, on the material to which the GaAs becomes attached. Mechanical modeling of the various GaAs assemblies has corroborated that mismatch in the coefficient of thermal expansion (CTE) between the GaAs MMIC and the material to which it is attached can cause minute anomalies present at chip processing to propagate into full-fledged failures at assembly and environmental conditioning.

The following evaluation examines both assembly and long-term reliability effects of GaAs MMIC solder attachment to a broad range of materials with CTEs from 5.1 ppm/ $^{\circ}$ C to 16.5 ppm/ $^{\circ}$ C. Some materials are standard carrier and housing base plate materials such as Kovar and Cu, others are more exotic metal matrix and metal infiltrated materials newly developed in the packaging industry.

**EXPERIMENTAL PROCEDURE**

GaAs devices were AuSn solder mounted to carrier and/or housing base plate materials utilizing a vacuum reflow processing technique. This process delivers a void-free attachment on most standard production materials. X-rays of all assemblies were completed after the reflow step. After the soldering operation and x-ray, samples were subjected to thermal cycling at -55 to +125 $^{\circ}$ C for 1000 cycles. Fractures were tabulated at specific intervals between 50 and 1000 cycles. Because of material availability, the reliability evaluation was undertaken in two time intervals. Phase 1 of the qualification included the materials Kovar, AlSi (60/40), CuMo (15/85), and CuW (10/90). Phase 2 testing expanded the tests to include AlSiC 55 percent, Copper, Al/AlN 40 percent and 50 percent, and AlGr discontinuous fiber. Kovar was utilized as a control in both tests. However, since a greater than expected number of cracks were experienced on the Kovar assemblies in Phase 1 of the qualification, in Phase 2 the Kovar assemblies were furnace reflowed to examine effects with a standard reflow technique which already has a good backup of historical data and experience. A sample of the reflowed assemblies is seen in Figure 1. Figure 2 shows one of the x-rays of the CuMo assemblies vacuum reflowed. The voids in the x-ray appear in black. The white areas are vias in the device which have filled with solder.

**RESULTS AND DISCUSSION**

Phase 1 vacuum reflow was accomplished with a peak temperature of 320 $^{\circ}$ C. In each case, two devices and two 0.010-inch-thick ceramic substrates were reflowed on each carrier. The carriers were 0.015 inch thick. Total number of reflowed devices for the Phase 1 testing was 40 on four different types of carrier plate materials. After reflow, the carrier plates were x-rayed and then submitted to thermal cycling of -55 to +125 $^{\circ}$ C according to MIL-STD-883 testing method 1010 condition B. The devices were removed and checked for fractures and chips initially prior to temperature cycle, and at 50, 200, and 1000 cycles. Tabulated results with respective material CTEs, as published by the suppliers, are shown in Table I. No fractures were seen in any devices at 50 cycles. At 200 cycles two devices mounted on Kovar carrier plates had propagated cracks. At 1000 cycles every device mounted on Kovar had fractured. None of the devices on AlSi (60/40), CuMo (15/85) or CuW (10/90) had cracks. X-ray

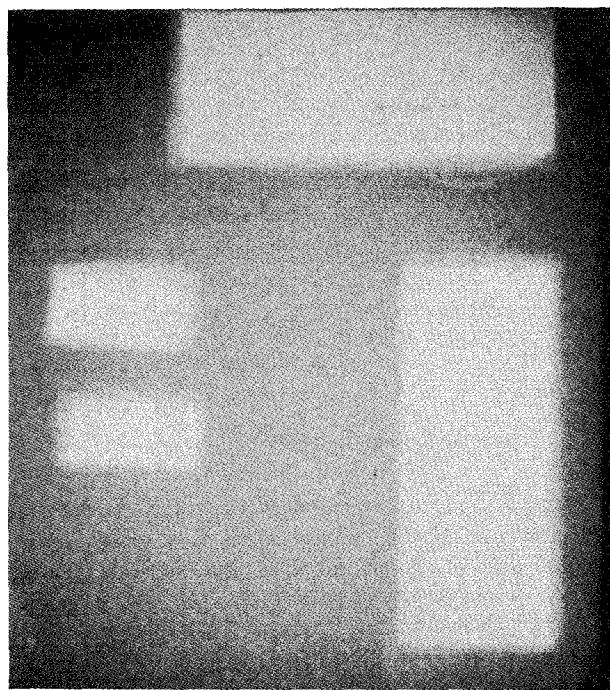
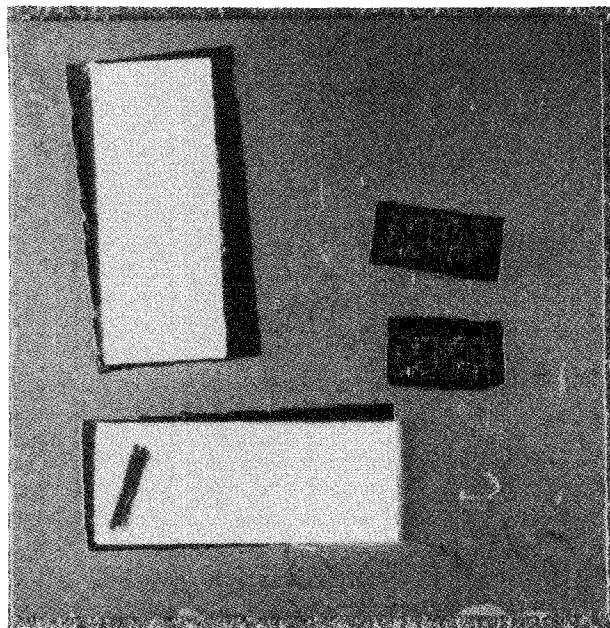


Figure 2. X-Ray of Two GaAs Devices and Two Thin Film Ceramics AuSn Vacuum Reflowed on a Copper Molybdenum Carrier

voiding levels were <0.5 percent on Kovar, CuMo, and CuW. On AlSi 10 percent voiding levels were seen attributable to inconsistencies in the plating of the carrier plates. No fractures were experienced on any of the ceramic substrates.

Although excellent attachment was experienced with devices mounted on the Kovar carrier plates, the worst

TABLE I. REFLOW RESULTS

Material	CTE ppm°C	Percent Cycles Fractured		
		50 Cycles	200 Cycles	1000 Cycles
CuMo	6.6	0	0	0
AlSi	10.5	0	0	0
CuW	6.5	0	0	0
Kovar	5.1	0	20	100

fracturing levels were demonstrated on this material. Modeling has verified that the level of tensile stress experienced will produce fracturing failures and that tensile stress is much more deleterious to long life reliability than compressive stress.

The Phase 2 testing broadened the range of materials under evaluation as noted above in the experimental procedure. As in the Phase 1 part of the qualification, the devices were reflowed with the vacuum reflow process (with the exception of devices mounted on Kovar carriers) at 320°C. After reflow the samples were x-rayed and submitted to thermal cycling at -55 to +125°C MIL-STD-883 method 1010 test condition B. The samples were examined initially and at 100, 500, and 1000 cycles. Table II lists the average number of voids, the CTE as published by the material supplier, and percent of devices fractured at 100, 500 and 1000 cycles.

The high level of voiding experienced with AlSiC and with AlGr has contributed to the fracturing seen on these materials. Materials with higher CTEs with respect to the CTE of GaAs such as copper, AlSi, and Al/AlN 40 percent actually experienced less fracturing than AlSiC. In addition to cracks through the device, however, another failure mode which was exhibited was fracturing of the corners. Prior tests with GaAs mounted to aluminum with a CTE of 23.5 ppm°C demonstrated that materials such as Al with high CTEs relative to the CTE of GaAs were likely to cause a significant number of fractures through the device as well as corners which cracked off. Table III shows corner damage which was incurred at 100, 500, and 1000 cycles.

Although no internal device fractures were exhibited in materials such as copper with a CTE of 16.5 ppm°C, 25 percent corner fractures resulted in classifying this material as unacceptable for GaAs solder mount. Since voiding levels with the copper was <0.5 percent, it is probable that the failure was caused by CTE mismatch between the copper and the GaAs as was seen with aluminum. Examining a material with CTE slightly less than copper at 13.4 ppm°C (Al/AlN 40 percent), it can be seen that little to no failures were experienced with only one corner chip in 36 devices or in 144 corners. An examination of Phase 1 samples demonstrated that CTEs from 6.5 to 10.5 ppm°C (CuMo-AlSi) also do not show any failures at the corners. Materials such as Kovar, on the other hand, with a CTE less than that of GaAs (5.1 versus 5.7 ppm°C) had 60 percent of the devices with corner failures in spite of the good attachment level (<0.5 percent voids).

**TABLE II. PHASE 2 RELIABILITY QUALIFICATION**

Material	Thickness (In)	No. of Devices	Devices Fractured (%)			Average Voids (%)	CTE ppm/ $^{\circ}$ C
			100 Temperature Cycles	500 Temperature Cycles	1000 Temperature Cycles		
AISIC 55% JA218013 DWA	0.065	20	0	10	10	10 - 40	8.2
AISIC 55% ACMC	0.030	16	0	0	0	20 - 30	8.2
AISIC 55% JA218014 ACMC	0.030	20	0	0	5	20 - 30	8.2
Copper	0.030	20	0	0	0	0.5	16.5
Al/AlN 40% JA216015 ACMC	0.030	20	0	0	0	1	13.4
Al/AlN 40% JA218016 ACMC	0.030	16	0	0	0	0.5	13.4
AlGr Discontinuous ACMC	0.030	17	30	35	35	50 - 60	9.2
Al/AlN 50% JA216012 ACMC	0.085	20	5	5	5	0.5	11.8
Kovar Furnace Reflowed	0.030	20	15	15	15	2 - 5	5.1

**TABLE III. CORNER DAMAGE**

Material	Percent Devices with Corner Fractures		
	100 Cycles	500 Cycles	1000 Cycles
AISic 55% DWA	35	35	70
AISic 55% ACMC	25	25	31
AISic 55% ACMC JA218014	20	25	25
Copper	25	25	25
Al/AlN 40 Percent JA218015	5	5	5
Al/AlN 40 Percent JA218016	0	0	0
AlGr Disc.	0	0	0
Al/AlN 50 Percent	20	20	20
Kovar Furnace Refl.	20	20	20

**CONCLUSION**

An evaluation/qualification was undertaken to examine reliability effects of GaAs solder attachment to a variety of different materials with a diverse range of coefficients of thermal expansion. Failure mechanisms included fractures or cracks through the devices as well as cracking of the corners. GaAs devices placed under tensile stress with materials such as Kovar (CTE 5.1 ppm/ $^{\circ}$ C) experienced severe cracking and corner fracture through long term reliability screening. Devices placed under compressive stress, on the other hand, did not degrade through life testing unless the CTE mismatch was greater than or equal to 16.5 ppm/ $^{\circ}$ C. From this evaluation, a coefficient of thermal expansion range was defined at which GaAs can be reliably attached and expected to operate without failures through 1000 cycles of MIL-STD thermal cycling.

**REFERENCES**

1. Lee, Chin C. and Goran S. Matuasevic, "Highly Reliable Die Attachment on Polished GaAs Surfaces Using Gold-Tin Eutectic Alloy." *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. Vol. 12, No. 3, September 1989.

2. Pavio, Jeanne S., "Successful Alloy Attachment of GaAs MMIC's." *IEEE Transactions on Microwave Theory and Techniques*. Vol. Mtt-35, No. 12, December 1987.
3. Soane, David S., "Stresses in Packaged Semiconductor Devices." *Solid State Technology*. May 1989.

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